UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

Vervain, LLC Plaintiff, v. Micron Technology, Inc.; Micron Semiconductor Products, Inc.; and Micron Technology Texas, LLC Defendants.	Civil Action No. 6:21-cv-487 JURY TRIAL DEMANDED

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Vervain, LLC ("Vervain") asserts the following claims for patent infringement against Defendants Micron Technology, Inc.; Micron Semiconductor Products, Inc.; and Micron Technology Texas, LLC (collectively "Micron" or "Defendants"), and alleges as follows.

NATURE OF THE ACTION

1. This is a civil action for infringement under the patent laws of the United States of America, 35 U.S.C. § 1 *et seq.*

2. Vervain is the owner of all rights, title, and interest in U.S. Patent Nos. 8,891,298; 9,196,385; 9,997,240; and 10,950,300 (collectively, the "Asserted Patents").

3. Defendants have infringed and continue to infringe one or more claims of Vervain's Asserted Patents by making, using, offering to sell, and selling within the United States, and importing into the United States, including in this District, certain flash memory products. Vervain seeks injunctive relief and monetary damages.

THE PARTIES

4. Plaintiff Vervain is a Texas limited liability company with its principal place of business located at 7424 Mason Dells Drive, Dallas, Texas 75230.

5. Defendant Micron Technology, Inc. ("Micron Technology") is a Delaware corporation with a principal place of business at 8000 South Federal Way, Boise, Idaho 83716. Micron Technology also has a place of business at 101 West Louis Henna Boulevard, Suite 210, Austin, Texas 78728. Micron Technology is registered with the Texas Secretary of State to do business in Texas.

6. Defendant Micron Semiconductor Products, Inc. ("Micron Semiconductor") is an Idaho corporation with a principal place of business at 8000 South Federal Way, Boise, Idaho 83716. Micron Semiconductor also has a place of business at 101 West Louis Henna Boulevard, Suite 210, Austin, Texas 78728. Micron Semiconductor is registered with the Texas Secretary of State to do business in Texas. Micron Semiconductor can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701-3218.

7. Defendant Micron Technology Texas, LLC ("Micron Texas") is an Idaho limited liability company with a principal place of business at 8000 South Federal Way, Boise, Idaho 83716. Micron Texas also has places of business at 101 West Louis Henna Boulevard, Suite 210, Austin, Texas 78728; and 805 Central Expressway South #100, Allen, Texas 75013. Micron Texas can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701-3218.

8. Micron produces computer memory and computer data storage including dynamic random access memory (DRAM), flash memory, USB flash drives, and other memory products. Micron's products are offered under the Micron, Crucial, and Ballistix brands, as well as private labels. Micron makes its own products in semiconductor fabrication plants in the United States

and other countries throughout the world. Micron sells its products to customers, including customers in this District, in the computer, networking and storage, consumer electronics, solid-state drives, and mobile telecommunications markets.

9. Micron maintains offices in Austin and Allen, Texas. Within the United States, Micron also has offices in Folsom, Irvine, Longmont, Milpitas, San Diego, and San Jose, California; Boise and Meridian, Idaho; Minneapolis, Minnesota; Lehi, Utah; Manassas, Virginia; and Seattle, Washington.[1] Outside the United States, Micron also has offices in China, India, Japan, Korea, Malaysia, Singapore, Taiwan, Belgium, Germany, Israel, Italy, and the United Kingdom.[2]

10. Micron operates semiconductor fabrication plants in Boise, Idaho; Lehi, Utah; and Manassas, Virginia, and fabricates and manufactures flash memory products in at least Manassas, Virginia.[3] Outside the United States, Micron operates semiconductor fabrication plants in at least China, Japan, Singapore, and Taiwan.[4]

11. Micron operates and owns the micron.com website, and markets, offers, distributes, and provides technical support for its flash memory products throughout the United States including in this District.

12. Each of the Defendants develops, designs, manufactures, distributes, markets, offers to sell, or sells infringing products or services within the United States, including in this District, and otherwise purposefully directs infringing activities to this District in connection

[1] Ex. E, https://www.micron.com/about/locations (printed March 12, 2021).
[2] *Id*.
[3] Ex. F, https://en.wikipedia.org/wiki/List_of_semiconductor_fabrication_plants (printed March 12, 2021).
[4] *Id*.

with its Austin, Texas office; its micron.com website; and its other places of business in Texas and the rest of the United States.

13. Defendants have been and are acting in concert, and are otherwise liable jointly, severally, or otherwise for relief related to or arising out of the same transaction, occurrence, or series of transactions or occurrences related to the making, using, selling, offering for sale, or otherwise distributing the flash memory products in this District.

14. In addition, this action involves questions of law and fact that are common to all Defendants. For example, Defendants are making, using, offering for sale, selling, or otherwise distributing at least some of the same flash memory products in this District.

JURISDICTION AND VENUE

15. This is a civil action for patent infringement arising under the patent laws of the United States, 35 U.S.C. § 1 *et seq*. This Court has subject matter jurisdiction over the matters asserted in this Complaint under 28 U.S.C. §§ 1331 and 1338(a) and 35 U.S.C. §§ 271 *et seq*.

16. This Court has personal jurisdiction over Defendants in accordance with due process and/or the Texas Long Arm Statute because, in part, Defendants "recruit[] Texas residents, directly or through an intermediary located in this state, for employment inside or outside this state." Tex. Civ. Prac. & Rem. Code § 17.042(3).

17. This Court has personal jurisdiction over Defendants, in part because Defendants do continuous and systematic business in this District, including by providing infringing products and services to residents of this District that Defendants knew would be used within this District, and by soliciting business from residents of this District.

18. For example, Defendants are subject to personal jurisdiction in this Court because, *inter alia*, they have regular and established places of business in this District, including

offices located at 101 West Louis Henna Boulevard, Suite 210, Austin, Texas 78728.[5] The Travis Central Appraisal District (CAD) website[6] indicates that both Micron Technology and Micron Semiconductor own property at 101 West Louis Henna Boulevard, Suite 210, Austin, Texas 78728, and that in 2020, it was appraised at more the $1.9 million dollars.[7]

19. Micron's Austin offices are regular and established places of business at least because these locations include many members of Micron's important teams, including storage system architects, SPME system architects, storage system engineers, storage solutions engineers, and software engineers. Micron posts job openings for its Austin office,[8] and as of March 12, 2021, Micron was posting five job openings for its Austin office that were available or recently filled.[9] These and additional job postings can be found on LinkedIn and various other websites.[10]

20. Based on publicly-available information, since 2012, Micron Technology has been the employer of approximately twenty-two recipients of H-1B visas who work and reside in

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[5] Ex. G, https://www.micron.com/about/locations?country=USA&city=Austin (printed March 12, 2021).
[6] https://www.traviscad.org/property-search/ (last visited March 12, 2021); http://propaccess.traviscad.org/clientdb/?cid=1 (last accessed March 12, 2021).
[7] Ex. H, http://propaccess.traviscad.org/clientdb/Property.aspx?prop_id=874673 (printed March 12, 2021) (property record for Micron Technology); http://propaccess.traviscad.org/clientdb/Property.aspx?prop_id=926072 (printed March 12, 2021) (property record for Micron Semiconductor).
[8] Ex. I, https://jobs.micron.com/search/?createNewAlert=false&q=&locationsearch=Austin (printed March 12, 2021).
[9] Ex. J, https://jobs.micron.com/job/Austin-Staff-Software-Engineer-TX-73301/711336000/ (printed March 26, 2021); Ex. K, https://jobs.micron.com/job/Austin-Principal-SystemSoftware-Architect-1-TX-73301/719885200/ (printed March 26, 2021); Ex. L, https://jobs.micron.com/job/Austin%2C-TX-Senior-Software-Engineer-TX-73301/718011200/ (printed March 26, 2021); Ex. M, https://jobs.micron.com/job/Austin-Senior-Competitive-Strategist-Storage-Business-Unit-TX-73301/715488100/ (printed March 26, 2021).
[10] Ex. N, https://www.linkedin.com/jobs/micron-technology-jobs-austin-texas-metropolitan-area?position=1&pageNum=0 (printed March 12, 2021); https://www.indeed.com/jobs?q=Micron+Technology&l=Austin%2C+TX (printed April 1, 2021).

the Austin, Texas area.[11] Micron Semiconductor has been the employer of at least two recipients of H-1B visas who work and reside in the Austin area.[12] Additionally, Micron Technology has been the employer of approximately seventeen recipients of H-1B visas who work and reside in the Allen, Texas area.[13]

21. Micron, directly and through agents, regularly conducts, solicits, and transacts business in this District and elsewhere in Texas, including through its micron.com website. For example, Defendants employ sales and marketing employees that regularly offer to sell, sell, or otherwise distribute flash memory products in this District and elsewhere in Texas.

22. In particular, Micron has committed and continues to commit acts of infringement in violation of 35 U.S.C. § 271, and has made, used, marketed, distributed, offered for sale, and sold infringing products in Texas, including in this District, and engaged in infringing conduct within and directed at or from this District. The infringing flash memory products have been and continue to be distributed to and used in this District. Micron's acts cause injury to Vervain, including injury suffered within this District.

23. Venue is proper in this District under 28 U.S.C. §§ 1391 and 1400(b) because a substantial part of the events or omissions giving rise to the claims occurred in this District, and because Defendants have committed acts of infringement in this District and have a regular and established place of business in this District.

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[11] Ex. O, https://h1bdata.info/index.php?em=Micron+Technology&job=&city=Austin&year=All+Years (printed March 26, 2021); https://h1bdata.info/index.php?em=Micron+Technology&job=&city=ROUND+ROCK&year=All+Years (printed March 26, 2021).
[12] Ex. P, https://h1bdata.info/index.php?em=Micron+Semiconductor&job=&city=Austin&year=All+Years (printed March 26, 2021).
[13] Ex. Q, https://h1bdata.info/index.php?em=Micron+Technology&job=&city=Allen&year=All+Years (printed March 26, 2021).

24. In particular, Micron Technology, Micron Semiconductor, and Micron Texas have regular and established places of business located at 101 West Louis Henna Boulevard, Suite 210, Austin, Texas 78728. Furthermore, Micron Technology, Micron Semiconductor, and Micron Texas are all registered to do business in Texas.

25. Micron Semiconductor and Micron Texas are wholly owned subsidiaries of Micron Technology. Micron Technology does not separately report revenue from Micron Semiconductor or Micron Texas in its filings to the Securities Exchange Commission, but rather reports combined revenue from its various products and subsidiaries.

26. On information and belief, Micron Technology not only "owns" but also "operates" Micron Semiconductor and Micron Texas, including the cooperative development, improvement, and support of Micron's products and services.

VERVAIN'S ASSERTED PATENTS

27. U.S. Patent No. 8,891,298 (the "'298 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on November 18, 2014. A true and correct copy of the '298 patent is attached as Exhibit A to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '298 patent, with the full and exclusive right to bring suit to enforce the '298 patent, including the right to recover for past infringement. The '298 patent is valid and enforceable under United States patent laws.

28. U.S. Patent No. 9,196,385 (the "'385 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on November 24, 2015. A true and correct copy of the '385 patent is attached as Exhibit B to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '385 patent, with the full and exclusive right to bring suit to enforce the '385 patent, including the right to recover for past infringement. The '385 patent is valid and enforceable under United States patent laws.

29. U.S. Patent No. 9,997,240 (the "'240 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on June 12, 2018. A true and correct copy of the '240 patent is attached as Exhibit C to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '240 patent, with the full and exclusive right to bring suit to enforce the '240 patent, including the right to recover for past infringement. The '240 patent is valid and enforceable under United States patent laws.

30. U.S. Patent No. 10,950,300 (the "'300 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on March 16, 2021. A true and correct copy of the '300 patent is attached as Exhibit D to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '300 patent, with the full and exclusive right to bring suit to enforce the '300 patent, including the right to recover for past infringement. The '300 patent is valid and enforceable under United States patent laws.

31. G.R. Mohan Rao is the sole inventor of the Asserted Patents.

32. Dr. Rao is the inventor of approximately 111 U.S. patents and the author of at least 15 technical publications spanning several decades.

33. Dr. Rao has been an innovator in the semiconductor industry since the 1960s. After receiving his Ph.D. in physics with a specialization in electronics in September 1968 from Andhra University in Waltair, India, near the village where he grew up, Dr. Rao traveled to the United States to attend a graduate program in physics at the University of Cincinnati, fulfilling his lifelong dream to study in the United States.

34. Shortly after beginning his studies at the University of Cincinnati, Dr. Rao found a bulletin indicating that Prof. William Carr of Southern Methodist University (SMU) was looking for a graduate assistant for his work on MOS transistors. Dr. Rao called Prof. Carr about

the opportunity, and by December 1968, after completing the fall semester at the University of Cincinnati, Dr. Rao had received the assistantship with Prof. Carr, moved to Dallas, Texas, and enrolled in a Ph.D. program at SMU in electrical engineering.

35. At the laboratory at SMU, Dr. Rao was able to build MOS devices from scratch. In the 1969-1970 timespan, while attending SMU, Dr. Rao also worked in the SMU laboratory with Jack Kilby of Texas Instruments, a pioneering electrical engineer who would later receive a Nobel Prize for his work. In early 1972, Mr. Kilby set up an interview for Dr. Rao at Texas Instruments' Houston facility, then the home of Texas Instruments' MOS-related work.

36. Dr. Rao began working for Texas Instruments in June 1972. He would go on to work for the company for 22 years, until 1994. Dr. Rao rose through the ranks at Texas Instruments, starting in an Engineer position and ascending to the position of Senior Fellow—one of 12 out of approximately 20,000 engineers at the company at the time. He then moved into a management position, starting as a Vice President in 1983 and becoming a Senior Vice President in 1985.

37. Dr. Rao received his first patent while working in a process and product engineering capacity to solve a production problem with Texas Instruments' 4-kilobit RAM product. From the late 1970s through the mid-1980s, he worked on and/or managed Texas Instruments': (1) 64Kb RAM, in a project management capacity as a Senior Member of Technical Staff; (2) 256Kb RAM, in a project management capacity as a Fellow; (3) 1Mb RAM, in a management capacity as a Senior Fellow, overseeing several projects; and (4) 4Mb RAM, in a management capacity as a Senior Fellow, overseeing several projects. At Texas Instruments, Dr. Rao also worked on projects involving EEPROM, SRAM, and microcontrollers. In total, Dr. Rao received approximately 35 U.S. patents during his time at Texas Instruments.

38. Some of Dr. Rao's work for Texas Instruments is featured in the Smithsonian Institution, in the Texas Instruments Collection.[14] For example, the Smithsonian Institution has a display of Texas Instruments' experimental 1-megabit CMOS DRAM with one-micron feature size, produced in April 1985 under Dr. Rao's leadership.

39. After his time at Texas Instruments, Dr. Rao joined Cirrus Logic in 1994. Although Cirrus Logic was a California company, Dr. Rao coordinated a team in the Dallas area. His work focused on a major project involving integration of a graphics controller and memory. During his time at Cirrus Logic, Dr. Rao received approximately 22 U.S. patents relating to his work on integrated graphics controllers and memory. Dr. Rao left Cirrus Logic in the summer of 1996.

40. Later in 1996, Dr. Rao started a company called Silicon Aquarius. Through a relationship between Silicon Aquarius and Matsushita, Dr. Rao led a design team in working on a 256Mb DRAM chip.

41. After Silicon Aquarius ceased operations, Dr. Rao did consulting work for a number of different companies and devoted much of his free time to thinking about various challenges and problems with which the semiconductor industry had struggled for years. For example, Dr. Rao worked to improve non-volatile memories that are used for long term storage of data after the power is turned off, and how to reduce the power consumption of those devices.

42. In non-volatile memories, there are two types of storage cells: single-level cells (SLCs) that store one bit of information, and multi-level cells (MLCs) that store multiple bits of information. SLCs are faster, more reliable, and have a longer life. MLCs are less expensive

[14] http://smithsonianchips.si.edu/texas/t_360.htm (last visited Apr. 12, 2021); http://smithsonianchips.si.edu/texas/wafer.htm (last visited Apr. 12, 2021).

and can store more data in less space with less power consumption. While working to improve these non-volatile memories, Dr. Rao developed inventions that combine the long life and high-performance of SLCs with the more cost-effective MLCs. The result is the best of both types of cells – longer life and better performance at less cost. By using the MLCs as the default storage, the cheaper, more reliable MLCs are used for the bulk of the data storage. Meanwhile, the SLCs are used for the data that needs it the most.

43. The claims of the Asserted Patents are directed to patent-eligible, non-abstract ideas. They address, among other things, specific improvements for controlling non-volatile memory modules. The claims are particularly useful for flash memory products or other memory devices that use a combination of SLCs and multi-level cells MLCs. If, for example, a range of addresses in a MLC memory module fails a data integrity test, the range of addresses may be mapped to a new range of addresses in a SLC memory module. Also, if a block in the MLC module is used frequently, the block may be transferred to the SLC module. By doing so, the reliability and life of the flash memory is increased.

44. Vervain's Asserted Patents claim, among other things, a specific implementation of a solution to a problem in the design and fabrication of flash memories. For example, the patents identify numerous specific advantages that Vervain's claimed techniques provide compared to traditional forms of flash memories. *See, e.g.*, Ex. A, '298 patent at 1:25-32; Ex. B, '385 patent at 1:28-35; Ex. C, '240 patent at 1:40-47; Ex. D, '300 patent at 1:44-51. Further, the claimed technologies cannot be performed as mental steps by a human, nor do they represent the application of a generic computer to any well-known method of organizing human behavior.

45. The Asserted Patents claim inventive concepts that are significantly more than any patent-ineligible, abstract idea. In particular, the claimed technologies, including individual

limitations as well as ordered combinations of limitations, were not well-understood, routine, or conventional, and cover multiple advantages, and combinations of advantages, that were not well-understood, routine, or conventional. *See, e.g.*, Ex. A, '298 patent at 5:24-40, 6:24-35; Ex. B, '385 patent at 5:28-44, 6:28-39; Ex. C, '240 patent at 5:43-59, 6:46-58; Ex. D, '300 patent at 5:51-67, 6:53-65.

DEFENDANTS' INFRINGING PRODUCTS AND ACTIVITIES

46. Micron is a global manufacturer and supplier of memory products, including non-volatile memory products. [15]

47. Micron's Compute and Networking Business Unit designs, makes, uses, offers to sell, sells, imports, supplies, or otherwise distributes memory products for client, cloud server, enterprise, graphics, and networking chips for cloud server, enterprise, client, graphics, and networking purposes.[16]

48. Micron's Mobile Business Unit designs, makes, uses, offers to sell, sells, imports, supplies, or otherwise distributes memory products for smartphones and other mobile-devices.[17]

49. Micron's Storage Business Unit designs, makes, uses, offers to sell, sells, imports, supplies, or otherwise distributes memory products for enterprise and cloud, client, and consumer storage purposes.[18]

50. Micron's Embedded Business Unit designs, makes, uses, offers to sell, sells, imports, supplies, or otherwise distributes memory products for industrial, automotive, and consumer markets.

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[15] Micron's 2020 Annual Report, available at http://www.annualreports.com/Company/micron-technology-inc (last visited April 5, 2021), at 4.
[16] *Id*.
[17] *Id*. at 5.
[18] *Id*. at 6.

51. Micron designs, makes, uses, offers to sell, sells, imports, supplies, or otherwise distributes, and provides support for, flash memory products, including products with the part name or number M600 SATA SSD, 2200 SSD, 2210 SSD, and 2300 SSD, and other memory products that have the same or similar structures, features, or functionalities, as the aforementioned products ("Accused Products").

52. The Accused Products are integrated into devices made, used, offered for sale, sold, imported, supplied, or otherwise distributed in the United States by among others, Micron, Micron's customers, original equipment manufacturers ("OEMs"), original design manufacturers ("ODMs"), foundry suppliers, distributers, and other third parties. Micron's Accused Products are essential, non-trivial components of the products into which they are integrated.

53. Micron also conducts research, development, and testing of Accused Products in the United States.

54. Micron maintains a website that advertised and continues to advertise the Accused Products, including identifying the applications for which they can be used and specifications for the Accused Products.

55. Micron's development, sales, marketing, and manufacturing activities in the United States, including within this District, directly contributed to Micron's net revenue in the United States.

COUNT I: INFRINGEMENT OF U.S. PATENT NO. 8,891,298

56. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

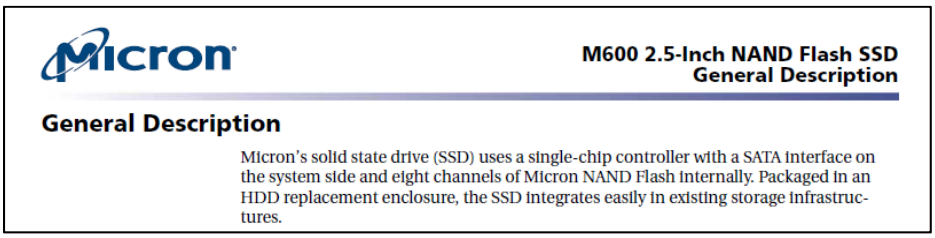
57. Defendants have directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '298 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35

U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

58. The Accused Products meet all the limitations of at least claim 1 of the '298 patent. Specifically, claim 1 of the '298 patent recites:

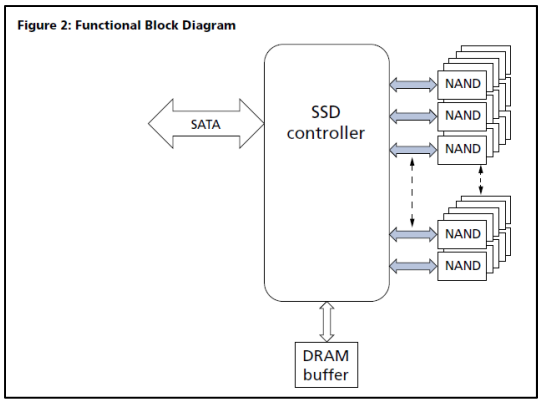
> A system for storing data comprising:
>
> at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;
>
> at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and
>
> a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to:
>
> a) maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;
>
> b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;
>
> c) determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed; and
>
> d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.

59. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, Micron's M600 SATA SSD ("M600") is a solid state drive (SSD) for storing data.



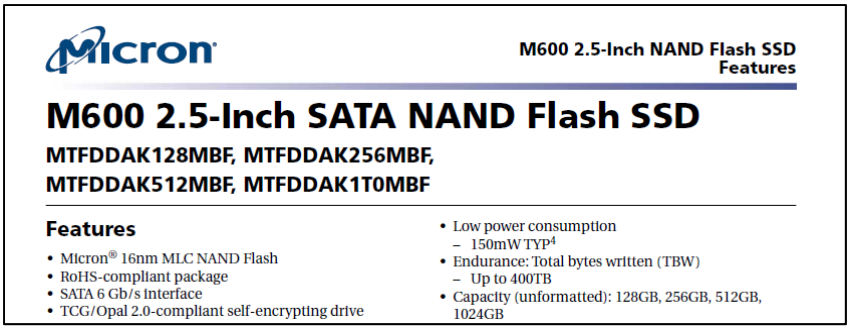
Data Sheet at 3[19]; *M600 Review*[20]; *SSDs for Big Data* at 1.[21]

60. The Accused Products include at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. For example, the M600 contains MLC NAND flash technology.



Data Sheet at 3.

[19] Ex. R, Micron's M600 Data Sheet ("*Data Sheet*"), available at https://media-www.micron.com/-/media/client/global/documents/products/data-sheet/ssd/m600_2_5_ssd.pdf?rev=ead5eb20949d47fcbbeb52e56ace0297 (last visited April 5, 2021).
[20] Ex. S, Micron M600 SSD Review ("*M600 Review*"), available at https://www.storagereview.com/review/micron-m600-ssd-review (last visited April 5, 2021).
[21] Ex. T, Micron Technical Marketing Brief, SSDs for Big Data – Fast Processing Requires High-Performance Storage ("*SSDs for Big Data*"), available at https://media-www.micron.com/-/media/client/global/documents/products/technical-marketing-brief/brief_ssds_big_data.pdf?rev=f0f0d0ba8773417988b37a5f223c89a9 (last visited April 5, 2021).



M600 2.5-Inch NAND Flash SSD
Features

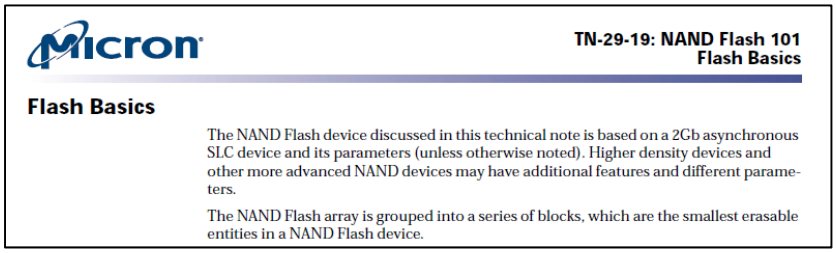
M600 2.5-Inch SATA NAND Flash SSD

MTFDDAK128MBF, MTFDDAK256MBF,
MTFDDAK512MBF, MTFDDAK1T0MBF

Features

- Micron® 16nm MLC NAND Flash
- RoHS-compliant package
- SATA 6 Gb/s interface
- TCG/Opal 2.0-compliant self-encrypting drive
- Low power consumption
  - 150mW TYP[4]
- Endurance: Total bytes written (TBW)
  - Up to 400TB
- Capacity (unformatted): 128GB, 256GB, 512GB, 1024GB

Id. at 1. The SSD is configured to erase MLC blocks.



TN-29-19: NAND Flash 101
Flash Basics

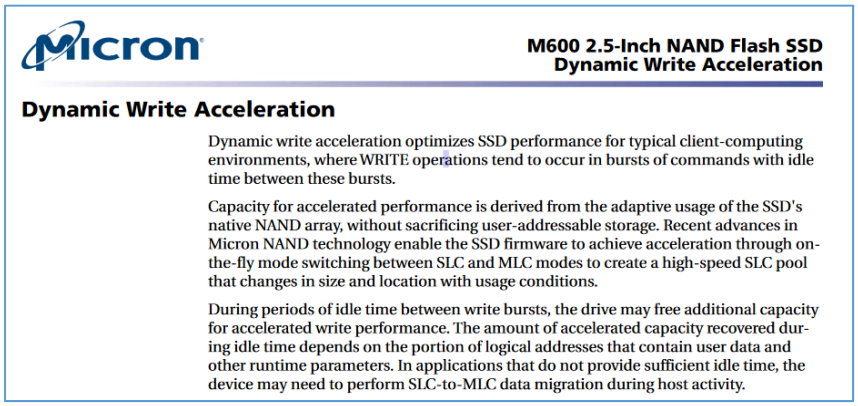
Flash Basics

The NAND Flash device discussed in this technical note is based on a 2Gb asynchronous SLC device and its parameters (unless otherwise noted). Higher density devices and other more advanced NAND devices may have additional features and different parameters.

The NAND Flash array is grouped into a series of blocks, which are the smallest erasable entities in a NAND Flash device.

Flash 101 at 2.[22]

61. The Accused Products include at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. For example, the M600 is configured to erase SLC blocks.



M600 2.5-Inch NAND Flash SSD
Dynamic Write Acceleration

Dynamic Write Acceleration

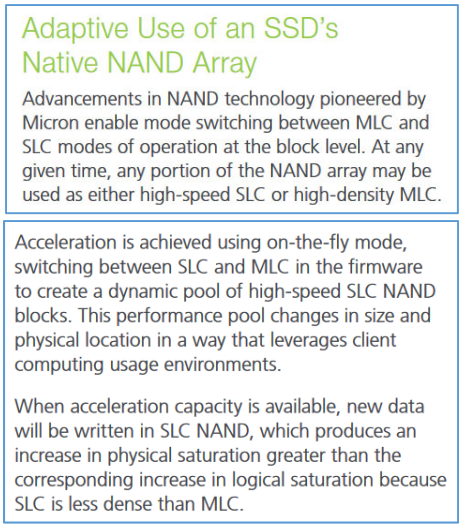
Dynamic write acceleration optimizes SSD performance for typical client-computing environments, where WRITE operations tend to occur in bursts of commands with idle time between these bursts.

Capacity for accelerated performance is derived from the adaptive usage of the SSD's native NAND array, without sacrificing user-addressable storage. Recent advances in Micron NAND technology enable the SSD firmware to achieve acceleration through on-the-fly mode switching between SLC and MLC modes to create a high-speed SLC pool that changes in size and location with usage conditions.

During periods of idle time between write bursts, the drive may free additional capacity for accelerated write performance. The amount of accelerated capacity recovered during idle time depends on the portion of logical addresses that contain user data and other runtime parameters. In applications that do not provide sufficient idle time, the device may need to perform SLC-to-MLC data migration during host activity.

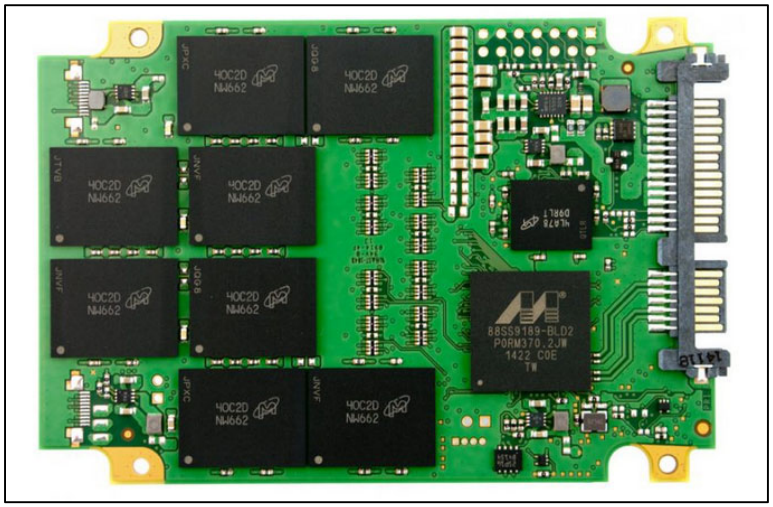
Data Sheet at 11.

[22] Ex. U, Micron Technical Note TN-29-19, NAND Flash 101: An Introduction to NAND Flash and How to Design It In to Your Next Product ("*Flash 101*"), available at https://www.micron.com/support/~/media/fea5cfd9ee9347f4b2afcd494d3291c3.ashx (last visited April 5, 2021).



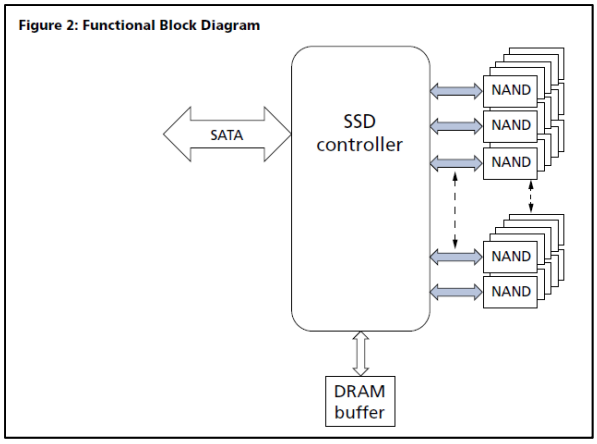
Write Acceleration at 1-2[23]; *Flash 101* at 2.

62. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module. For example, the M600 contains a controller with a NAND interface.

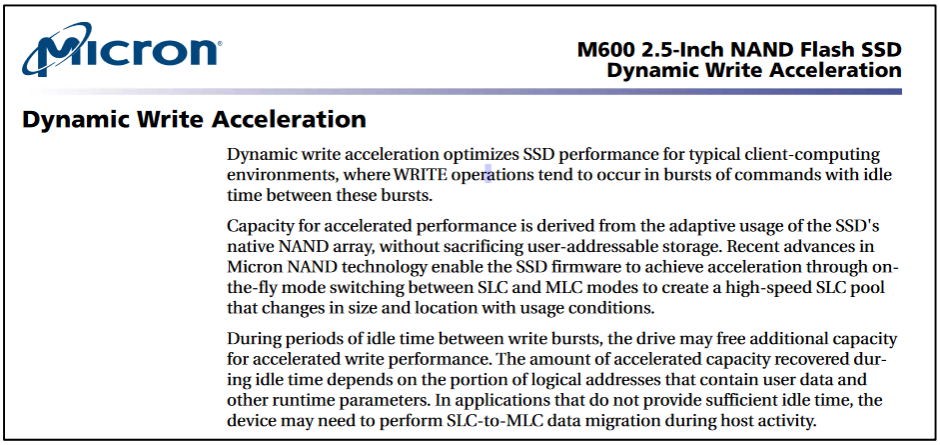


M600 Review.

[23] Ex. V, Micron Technical Marketing Brief, Optimized Client Computing with Dynamic Write Acceleration ("*Write Acceleration*"), available at https://www.micron.com/-/media/client/global/documents/products/technical-marketing-brief/brief_ssd_dynamic_write_accel.pdf (last visited April 6, 2021).



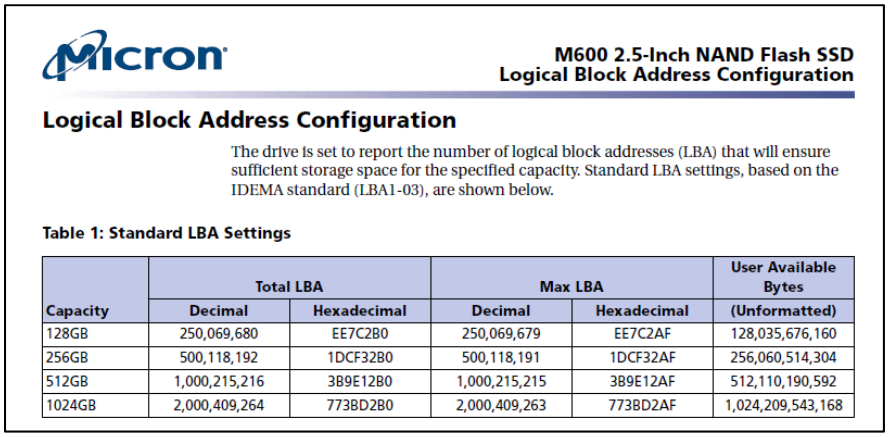
Data Sheet at 3.



Data Sheet at 11.

63. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. For example, the controller in the M600 uses a mapping

table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory.



M600 2.5-Inch NAND Flash SSD
Logical Block Address Configuration

Logical Block Address Configuration

The drive is set to report the number of logical block addresses (LBA) that will ensure sufficient storage space for the specified capacity. Standard LBA settings, based on the IDEMA standard (LBA1-03), are shown below.

Table 1: Standard LBA Settings

Capacity	Total LBA		Max LBA		User Available Bytes
	Decimal	Hexadecimal	Decimal	Hexadecimal	(Unformatted)
128GB	250,069,680	EE7C2B0	250,069,679	EE7C2AF	128,035,676,160
256GB	500,118,192	1DCF32B0	500,118,191	1DCF32AF	256,060,514,304
512GB	1,000,215,216	3B9E12B0	1,000,215,215	3B9E12AF	512,110,190,592
1024GB	2,000,409,264	773BD2B0	2,000,409,263	773BD2AF	1,024,209,543,168

Data Sheet at 4.

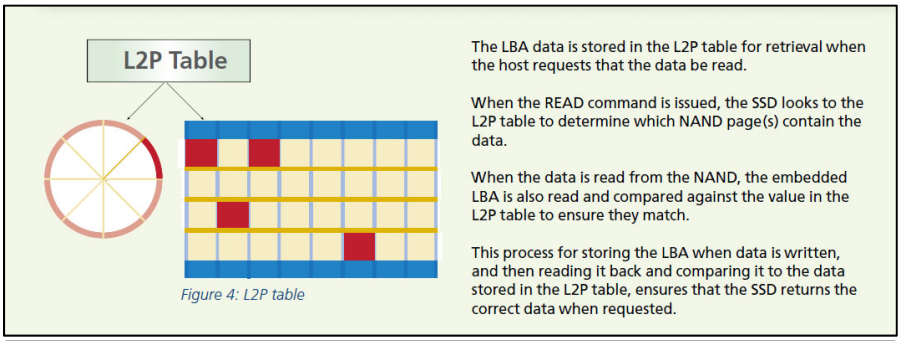


Figure 4: L2P table

The LBA data is stored in the L2P table for retrieval when the host requests that the data be read.

When the READ command is issued, the SSD looks to the L2P table to determine which NAND page(s) contain the data.

When the data is read from the NAND, the embedded LBA is also read and compared against the value in the L2P table to ensure they match.

This process for storing the LBA when data is written, and then reading it back and comparing it to the data stored in the L2P table, ensures that the SSD returns the correct data when requested.

This data structure is referred to as the L2P table.

Because the L2P table is stored in DRAM, the potential exists for data corruption within the table itself. The consequence of such corruption can be severe, with data loss being paramount.

Because of this potential, the L2P tables in all of Micron's RealSSD products are protected by parity. This parity check protection method provides an extremely robust structure.

When the host writes data to the SSD, two key elements combine: the actual data to be written and the LBA from which it came. For example, if the host data was a building, the LBA would be that building's street address. All data written to the SSD has an LBA associated with it. Micron embeds the host LBA, along with the user data it references, logically, joining them before writing anything to the NAND, as shown on the right.

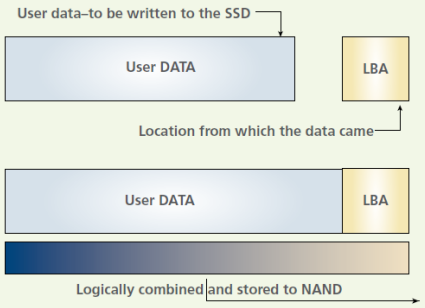
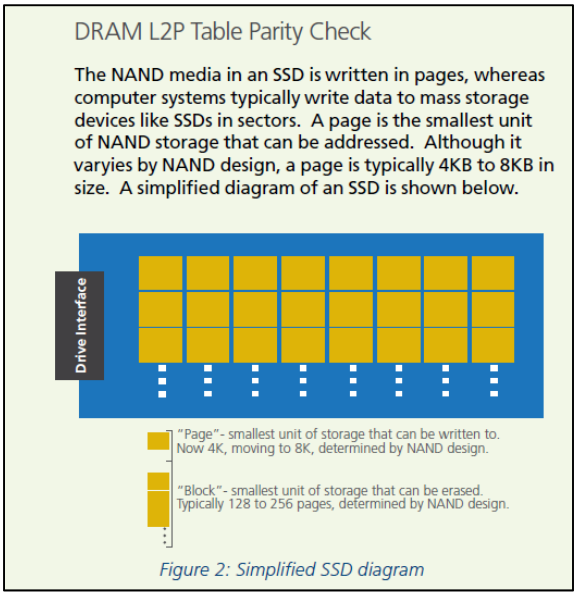


Figure 5: Writing data to the SSD

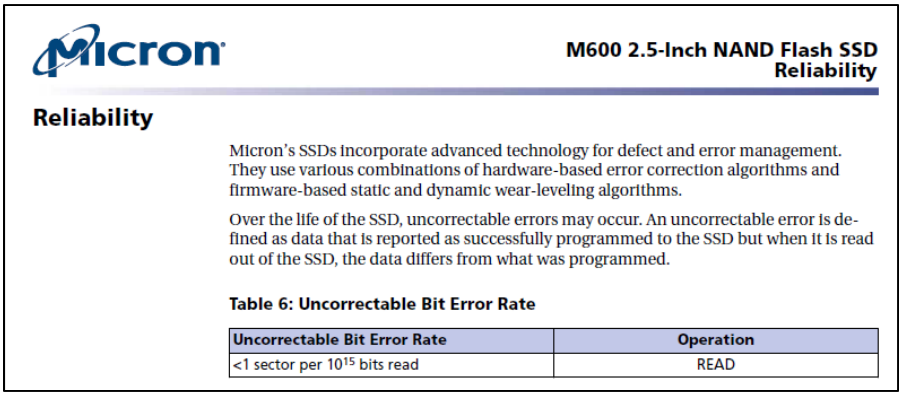
Protection at 3.[24] The flash memory is organized by page and block, where a page is the smallest program unit and a block is the smallest erase unit.



Id. at 2.

64. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. For example, the M600 incorporates defect and error management technology.

[24] Ex. W, Micron Technical Marketing Brief, A Comparison of Client and Enterprise SSD Data Path Protection ("*Protection*"), available at https://www.micron.com/-/media/client/global/documents/products/technical-marketing-brief/brief_ssd_datapath_protection_client_enterprise.pdf?la=en (last visited April 6, 2021).



M600 2.5-Inch NAND Flash SSD
Reliability

Reliability

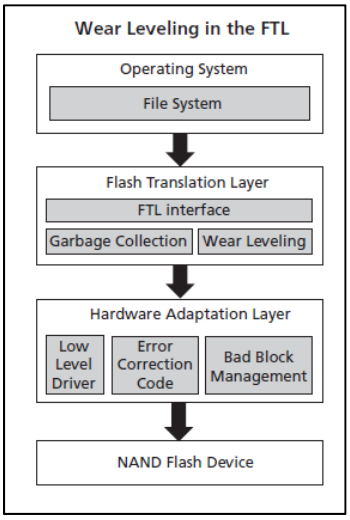
Micron's SSDs incorporate advanced technology for defect and error management. They use various combinations of hardware-based error correction algorithms and firmware-based static and dynamic wear-leveling algorithms.

Over the life of the SSD, uncorrectable errors may occur. An uncorrectable error is defined as data that is reported as successfully programmed to the SSD but when it is read out of the SSD, the data differs from what was programmed.

Table 6: Uncorrectable Bit Error Rate

Uncorrectable Bit Error Rate	Operation
<1 sector per 10^{15} bits read	READ

Data Sheet at 8.



Conclusion

Implementing wear leveling is recommended as part of the software tool chain (either in the FTL or file system) to increase the lifetime of NAND Flash in an embedded system.

In addition, it is recommended that you implement garbage collection and bad block management algorithms. It is mandatory that you implement error correction code algorithms.

To help integrate NAND Flash memory in applications, Micron can provide a full range of software solutions, such as a file system, sector manager, drivers, and code management. Contact your Micron sales representative or visit *www.micron.com* for more details.

Wear Leveling TN-29-61 at 2, 5.[25] The controller addresses data integrity issues by remapping data.

[25] Ex. X, Micron Technical Note TN-29-61, Wear Leveling in Micron NAND Flash Memory ("*Wear Leveling TN-29-61*"), available at https://www.micron.com/-/media/client/global/documents/products/technical-note/nand-flash/tn2961_wear_leveling_in_nand.pdf (last visited April 6, 2021).

Introduction

NAND Flash devices are no longer limited to mobile mass storage applications. They are being designed into increasingly complex and diverse systems to store operating systems and other critical data. Requirements for maintaining data integrity are more stringent for these applications than for mass storage devices. Even a single uncorrectable bit error that is not critical for many types of mass storage applications becomes a concern for embedded applications and other designs migrating to NAND Flash storage.

The host must implement application-level data management for NAND Flash to be an effective memory solution and for data integrity to be maintained. COPYBACK operations, which are sometimes referred to as INTERNAL DATA MOVE (IDM) operations, play a key role in maintaining data integrity in the NAND Flash device. This technical note describes how to use COPYBACK operations.

Preventing Data Errors in NAND Flash Devices

When moving data within a NAND Flash device, data errors can occur the same way they occur when the device is programmed and read. Some of the common mechanisms that cause data errors are described in Micron Technical Note TN-29-17: "NAND Flash Design and Use Considerations."

Because of these error mechanisms, all NAND Flash devices require error correction code (ECC). ECC helps protect against PROGRAM and READ errors. However, using COPYBACK operations without external data output (and data input, if required) can lead to errors beyond ECC protection limits. When the number of data errors exceeds ECC protection limits, data integrity is compromised, and application-level failures can occur.

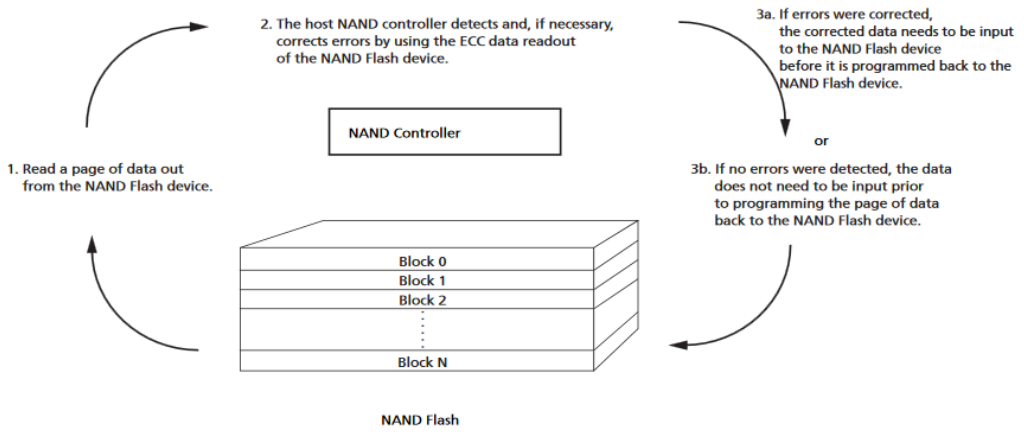
Inputting/Outputting Data During COPYBACK Operations

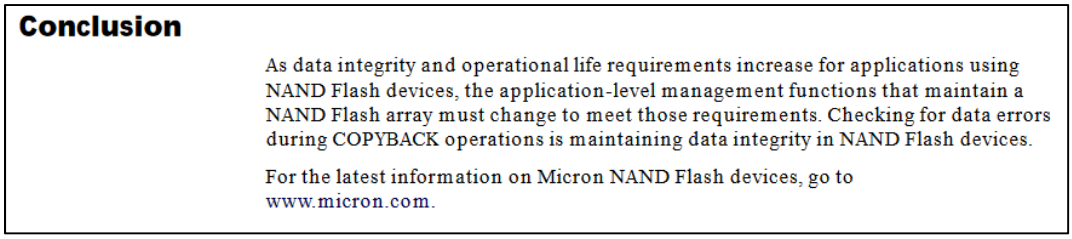
Using COPYBACK operations is the most efficient way to move data from one location to another within a NAND Flash device. When performing COPYBACK operations, data is not input or output external to the device. However, data integrity issues can occur if data input and output options are not used. Inputting and outputting data during COPYBACK operations enable data to be corrected and returned to its original programmed value, and it resets ECC to its maximum level of error correction capability. Resetting ECC also prevents the number of data errors from accumulating beyond the ECC error correction capability. This helps maintain data integrity over the operational life of the device.

When reading data out during COPYBACK operations, data errors can be detected by comparing READ data with ECC data. If data errors are detected, ECC data can be used to correct any bit errors within the ECC correction threshold prior to programming

(inputting) the data back into the NAND Flash device (as shown in Figure 1). If no data errors are detected, no data input is required. This method of checking and correcting data during COPYBACK operations minimizes the number of data errors occurring beyond the ECC error correction capability.

Figure 1: Flow for Maintaining Data Integrity via COPYBACK Operations





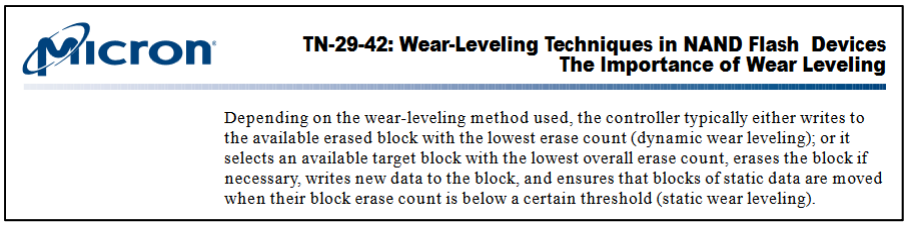
Conclusion

As data integrity and operational life requirements increase for applications using NAND Flash devices, the application-level management functions that maintain a NAND Flash array must change to meet those requirements. Checking for data errors during COPYBACK operations is maintaining data integrity in NAND Flash devices.

For the latest information on Micron NAND Flash devices, go to www.micron.com.

COPYBACK at 1-3.[26]

65. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed. For example, the M600 employs wear leveling techniques that employ block erase counting.



Micron

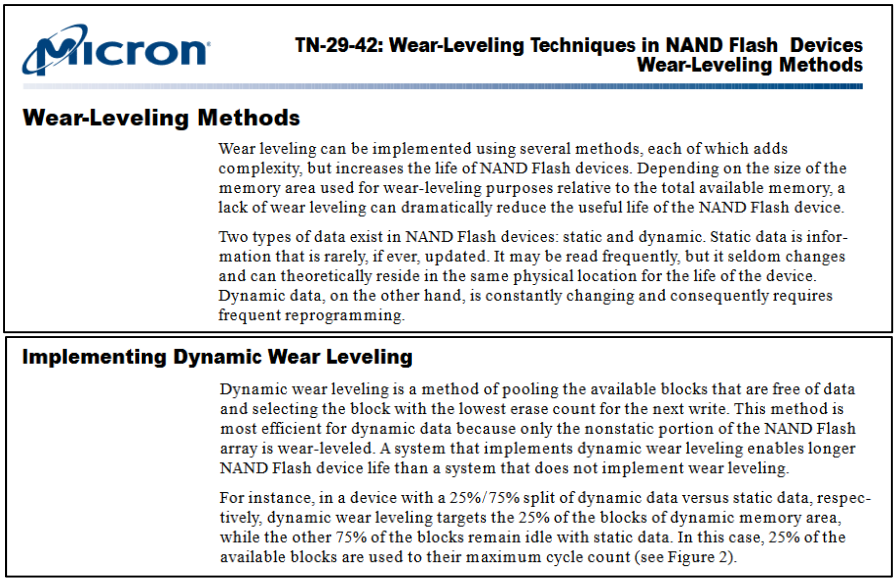
TN-29-42: Wear-Leveling Techniques in NAND Flash Devices
The Importance of Wear Leveling

Depending on the wear-leveling method used, the controller typically either writes to the available erased block with the lowest erase count (dynamic wear leveling); or it selects an available target block with the lowest overall erase count, erases the block if necessary, writes new data to the block, and ensures that blocks of static data are moved when their block erase count is below a certain threshold (static wear leveling).

Wear-Leveling TN-29-42 at 2.[27]

[26] Ex. Y, Micron Technical Note TN-29-41, Using COPYBACK Operations to Maintain Data Integrity in NAND Flash Devices ("*COPYBACK*"), available at https://media-www.micron.com/-/media/client/global/documents/products/technical-note/nand-flash/tn2941_idm_copyback.pdf?rev=c0a04e8ff8bd4f309bab7ea91ad98035 (last visited April 6, 2021).

[27] Ex. Z, Micron Technical Note TN-29-42, Wear-Leveling Techniques in NAND Flash Devices ("*Wear-Leveling TN-29-42*"), available at https://media-www.micron.com/-/media/client/global/documents/products/technical-note/nand-flash/tn2942_nand_wear_leveling.pdf (last visited April 6, 2021).



TN-29-42: Wear-Leveling Techniques in NAND Flash Devices
Wear-Leveling Methods

Wear-Leveling Methods

Wear leveling can be implemented using several methods, each of which adds complexity, but increases the life of NAND Flash devices. Depending on the size of the memory area used for wear-leveling purposes relative to the total available memory, a lack of wear leveling can dramatically reduce the useful life of the NAND Flash device.

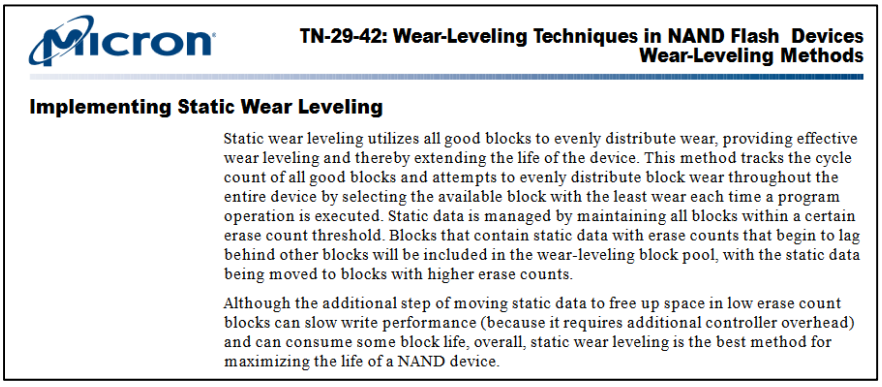
Two types of data exist in NAND Flash devices: static and dynamic. Static data is information that is rarely, if ever, updated. It may be read frequently, but it seldom changes and can theoretically reside in the same physical location for the life of the device. Dynamic data, on the other hand, is constantly changing and consequently requires frequent reprogramming.

Implementing Dynamic Wear Leveling

Dynamic wear leveling is a method of pooling the available blocks that are free of data and selecting the block with the lowest erase count for the next write. This method is most efficient for dynamic data because only the nonstatic portion of the NAND Flash array is wear-leveled. A system that implements dynamic wear leveling enables longer NAND Flash device life than a system that does not implement wear leveling.

For instance, in a device with a 25%/75% split of dynamic data versus static data, respectively, dynamic wear leveling targets the 25% of the blocks of dynamic memory area, while the other 75% of the blocks remain idle with static data. In this case, 25% of the available blocks are used to their maximum cycle count (see Figure 2).

Id. at 3.



TN-29-42: Wear-Leveling Techniques in NAND Flash Devices
Wear-Leveling Methods

Implementing Static Wear Leveling

Static wear leveling utilizes all good blocks to evenly distribute wear, providing effective wear leveling and thereby extending the life of the device. This method tracks the cycle count of all good blocks and attempts to evenly distribute block wear throughout the entire device by selecting the available block with the least wear each time a program operation is executed. Static data is managed by maintaining all blocks within a certain erase count threshold. Blocks that contain static data with erase counts that begin to lag behind other blocks will be included in the wear-leveling block pool, with the static data being moved to blocks with higher erase counts.

Although the additional step of moving static data to free up space in low erase count blocks can slow write performance (because it requires additional controller overhead) and can consume some block life, overall, static wear leveling is the best method for maximizing the life of a NAND device.

Id. at 4.

66. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module. For example, the M600 employs wear leveling techniques that transfer blocks within the flash memory. *Wear-Leveling TN-29-42* at 2-4.

67. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

68. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

69. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '298 patent by Defendants.

COUNT II: INFRINGEMENT OF U.S. PATENT NO. 9,196,385

70. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

71. Defendants have directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '385 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

72. The Accused Products meet all the limitations of at least claim 1 of the '385 patent. Specifically, claim 1 of the '385 patent recites:

> A system for storing data comprising:
>
> at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;
>
> at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a flash translation layer (FTL); wherein the FTL is adapted to:

a) maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;

b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

c) determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed; and

d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.

73. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, the M600 is a SSD for storing data. *Data Sheet* at 3; *M600 Review*; *SSDs for Big Data* at 1.

74. The Accused Products include at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. For example, the M600 contains MLC NAND flash technology. *Data Sheet* at 1, 3. The SSD is configured to erase MLC blocks. *Flash 101* at 2.

75. The Accused Products include at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. For example, the M600 is configured to erase SLC blocks. *Data Sheet* at 11; *Write Acceleration* at 1-2; *Flash 101* at 2.

76. The Accused Products include a flash translation layer (FTL). For example, the M600 contains a Flash Transition Layer (FTL). *Wear Leveling TN-29-61* at 1-2.

77. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. For example, the FTL in the M600 uses a mapping table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory. *Data Sheet* at 4; *Protection* at 3. The flash memory is organized by page and block, where a page is the smallest program unit and a block is the smallest erase unit. *Id*. at 2.

78. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. For example, the M600 incorporates defect and error management technology. *Data Sheet* at 8; *Wear Leveling TN-29-61* at 2, 5. The FTL addresses data integrity issues by remapping data. *COPYBACK* at 1-3.

79. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of

times each one of the blocks is accessed. For example, the M600 employs wear leveling techniques that employ block erase counting. *Wear-Leveling TN-29-42* at 2-4.

80. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module. For example, the M600 employs wear leveling techniques that transfer blocks within the flash memory. *Wear-Leveling TN-29-42* at 2-4.

81. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

82. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

83. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '385 patent by Defendants.

COUNT III: INFRINGEMENT OF U.S. PATENT NO. 9,997,240

84. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

85. Defendants have directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 6 of the '240 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing

activities, products, and services, including, for example, on the basis of information obtained during discovery.

86. The Accused Products meet all the limitations of at least claim 6 of the '240 patent. Specifically, claim 6 of the '240 patent recites:

> 6. A system for storing data comprising:
>
> at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;
>
> at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and
>
> a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;
>
> wherein the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and
>
> wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;
>
> wherein the controller is further adapted to maintain a count value of those blocks that are accessed most frequently and, on a periodic basis when the count value is a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller.

87. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, the M600 is a SSD for storing data. *Data Sheet* at 3; *M600 Review*; *SSDs for Big Data* at 1.

88. The Accused Products include at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. For example, the M600 contains MLC NAND flash technology. *Data Sheet* at 3. The SSD is configured to erase MLC blocks. *Flash 101* at 2.

89. The Accused Products include at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. For example, the M600 is configured to erase SLC blocks. *Data Sheet* at 11; *Write Acceleration* at 1-2; *Flash 101* at 2.

90. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. For example, the M600 contains a controller with a NAND interface. *M600 Review*; *Data Sheet* at 3, 11. The controller uses a mapping table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory. *Data Sheet* at 4; *Protection* at 3. The flash memory is organized by page and block, where a page is the smallest program unit and a block is the smallest erase unit. *Protection* at 2.

91. In the Accused Products, the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks. For example, the M600 employs wear leveling techniques that employ block erase counting. *Wear-Leveling TN-29-42* at 2-4.

92. In the Accused Products, the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. For example, the M600 incorporates defect and error management technology. *Data Sheet* at 6; *Wear Leveling TN-29-61* at 2, 5. The controller addresses data integrity issues by remapping data. *COPYBACK* at 1-3.

93. In the Accused Products, the controller is adapted to maintain a count value of those blocks that are accessed most frequently and, on a periodic basis when the count value is a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller. For example, the M600 employs wear leveling techniques that employ block erase counting, and that transfer blocks within the flash memory. *Wear-Leveling TN-29-42* at 2-4.

94. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain

reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

95. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

96. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '240 patent by Defendants.

COUNT IV: INFRINGEMENT OF U.S. PATENT NO. 10,950,300

97. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

98. Defendants have directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '300 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on reverse engineering reports currently available, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

99. The Accused Products meet all the limitations of at least claim 1 of the '300 patent. Specifically, claim 1 of the '300 patent recites:

> A system for storing data comprising:
>
> memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space;
>
> at least one controller to operate memory elements and associated memory space;
>
> at least one MLC nonvolatile memory element that can be mapped into the MLC memory space;

at least one SLC nonvolatile memory element that can be mapped into the SLC memory space;

at least one random access volatile memory;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory;

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;

the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation is performed thereon by comparing the stored data to the retained data in the random access volatile memory;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

100. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, the M600 is a SSD for storing data. *Data Sheet* at 3; *M600 Review*; *SSDs for Big Data* at 1.

101. The Accused Products include memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space. For example, the M600 contains DRAM memory space and MLC and SLC flash memory space. *Data Sheet* at 1, 3 & 11; *Write Acceleration* at 1-2; *Protection* at 1-5.

102. The Accused Products include at least one controller to operate memory elements and associated memory space. For example, the M600 contains a controller to operate memory elements and associated memory space. *M600 Review*; *Data Sheet* at 3, 11; *Protection* at 1-5.

103. The Accused Products include at least one MLC nonvolatile memory element that can be mapped into the MLC memory space. For example, the controller in the M600 uses a mapping table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory. *Data Sheet* at 4; *Protection* at 3. The flash memory contains MLC memory space. *Data Sheet* at 1, 3.

104. The Accused Products include at least one SLC nonvolatile memory element that can be mapped into the SLC memory space. For example, the controller in the M600 uses a mapping table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory. *Data Sheet* at 4; *Protection* at 3. The flash memory contains SLC memory space. *Data Sheet* at 3, 11; *Write Acceleration* at 1-2.

105. The Accused Products include at least one random access volatile memory. For example, the M600 contains DRAM memory. *Data Sheet* at 3; *Protection* at 1-5.

106. The Accused Products include an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory. For example, the controller in the M600 contains a FTL and uses a mapping table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory. *Wear Leveling TN-29-61* at 1-2; *Data Sheet* at 4; *Protection* at 3.

107. The Accused Products include a controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data

therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory. For example, the controller in the M600 controls access to the MLC and SLC memory and the DRAM. *Data Sheet* at 3. The controller stores data in the flash memory and retains data in the DRAM. *Protection* at 1, 3.

108. In the Accused Products, the controller performs a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation is performed thereon by comparing the stored data to the retained data in the random access volatile memory. For example, the controller in the M600 performs a data integrity test by comparing data stored in the flash memory with data retained in the DRAM. *Protection* at 1, 3.

109. In the Accused Products, the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories. For example, the M600 employs wear leveling techniques that transfer blocks within the flash memory. *Wear-Leveling TN-29-42* at 2-4; *Flash 101* at 2. The controller uses a mapping table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory. *Data Sheet* at 4; *Protection* at 3. The flash memory is organized by page and block, where a page is the smallest program unit and a block is the smallest erase unit. *Protection* at 2.

110. In the Accused Products, a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance. For

example, the M600 incorporates defect and error management technology. *Data* Sheet at 8; *Wear Leveling TN-29*-61 at 2, 5. The controller addresses data integrity issues by remapping data. COPYBACK at 1-3.

111. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

112. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

113. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '300 patent by Defendants.

REQUEST FOR A JURY TRIAL

114. Vervain requests a jury trial of all issues in this action so triable.

PRAYER FOR RELIEF

WHEREFORE, Vervain respectfully requests:

A. That Judgment be entered that Defendants have infringed one or more claims of the Asserted Patents, literally and under the doctrine of equivalents;

B. That, in accordance with 35 U.S.C. § 283, Defendants and all its affiliates, employees, agents, officers, directors, attorneys, successors, and assigns and all those acting on behalf of or in active concert or participation with any of them, be preliminarily and permanently enjoined from (1) infringing the Asserted Patents and (2) making, using, selling, and offering for sale, or importing into the United States, the Accused Products;

C. An award of damages sufficient to compensate Vervain for Defendants' infringement under 35 U.S.C. § 284;

D. That the case be found exceptional under 35 U.S.C. § 285 and that Vervain be awarded its reasonable attorneys' fees;

E. Costs and expenses in this action;

F. An award of prejudgment and post-judgment interest; and

G. Such other and further relief as the Court may deem just and proper.

Dated: May 10, 2021.

Respectfully submitted,

/s/ Alan L. Whitehurst

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